Development of Emulsion Readout System "Super UTS"

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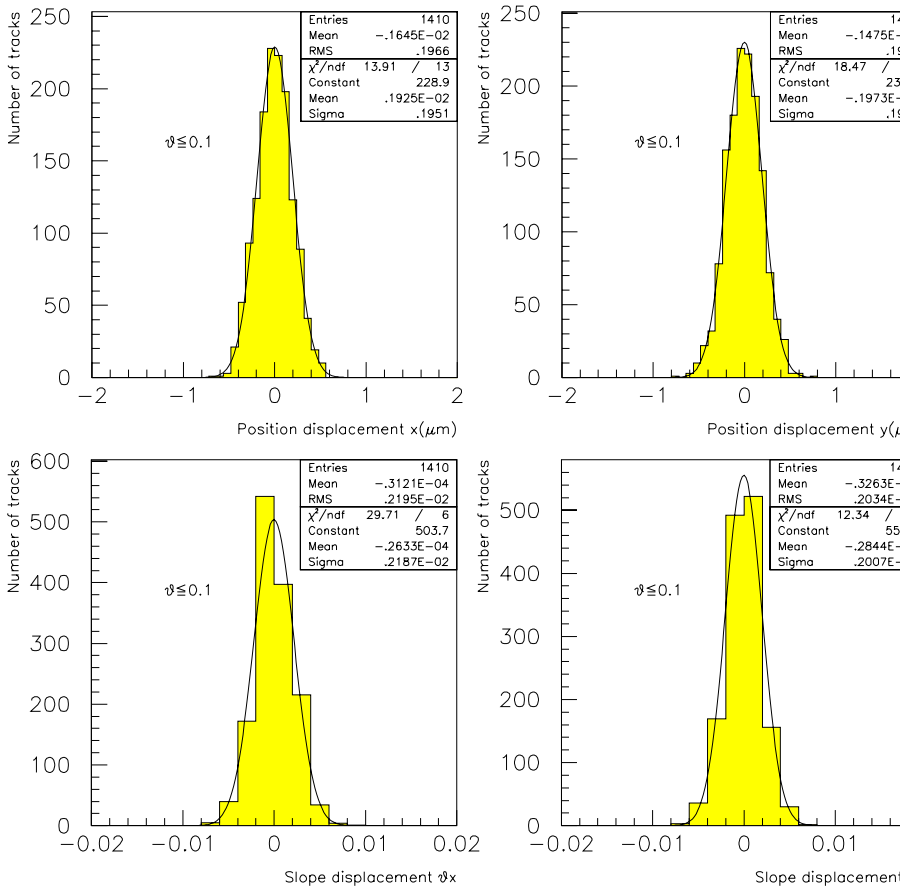
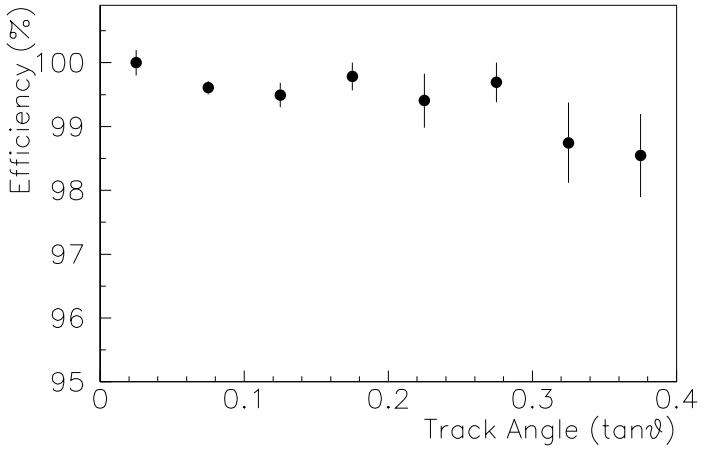
The Performance of Current Emulsion Readout System

- Position resolution
  σ~ **0.2 μm**
- Angle resolution
  σ~ **2 mrad**
- Efficiency **~99%**
- Scanning speed
  1cm²/hrs up to ±400mrad





Track recognition algorithm

- Take Tomographic Image with microscope
  - 16 images for 1 view data set. A few micron focal depth each
- Shifting image and make coincidence.

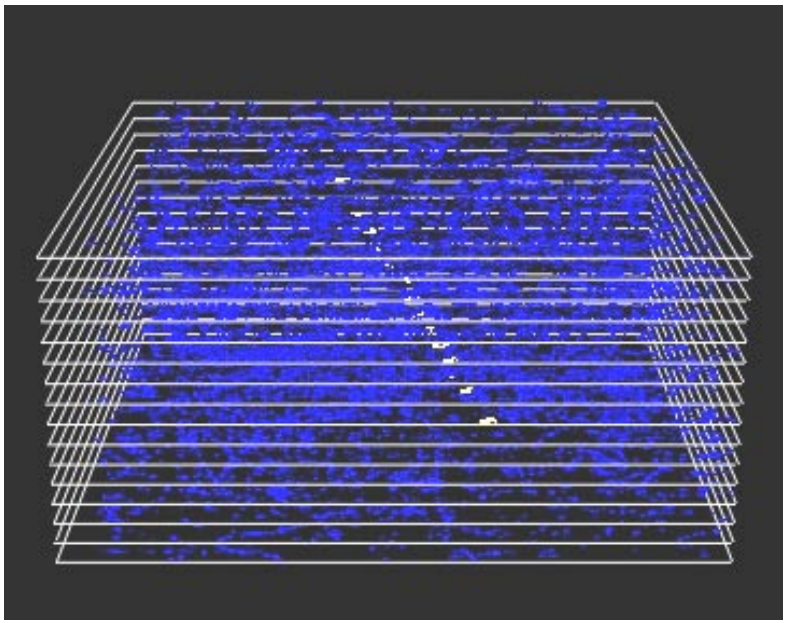
Invented in 1974
Established in 1985

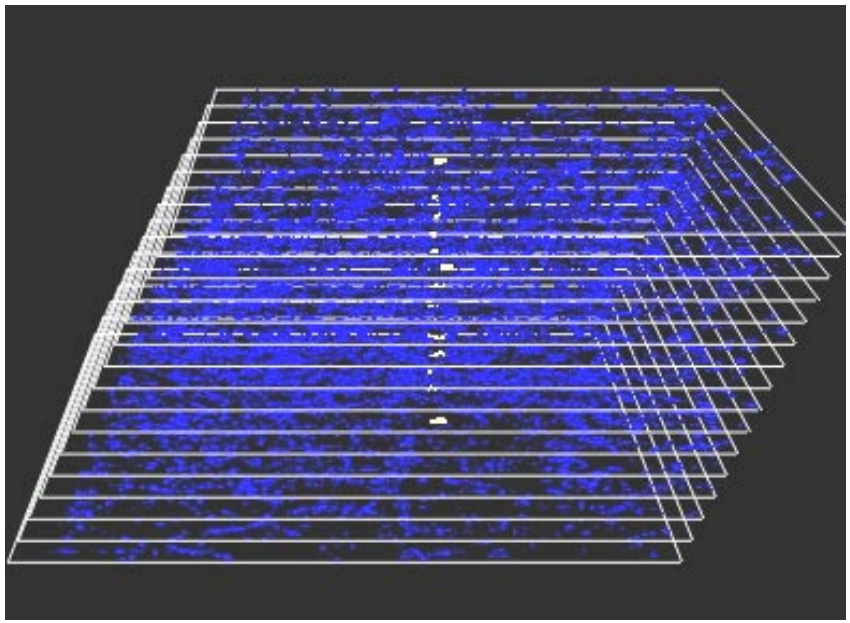
Easy to implement in Hardware

Optimum memory bandwidth can be designed.

Easy to estimate processing time.

Reasonable cost.





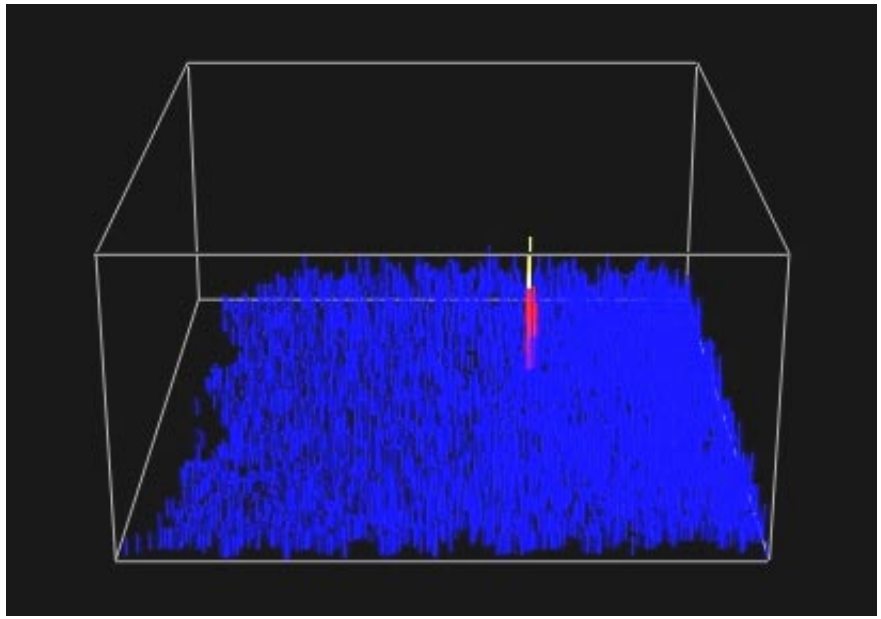
Repeat on angle space

Take 16 tomographic images

Shift images focusing an angle

Sum up all images to make coincidence

Appear tracks as peaks



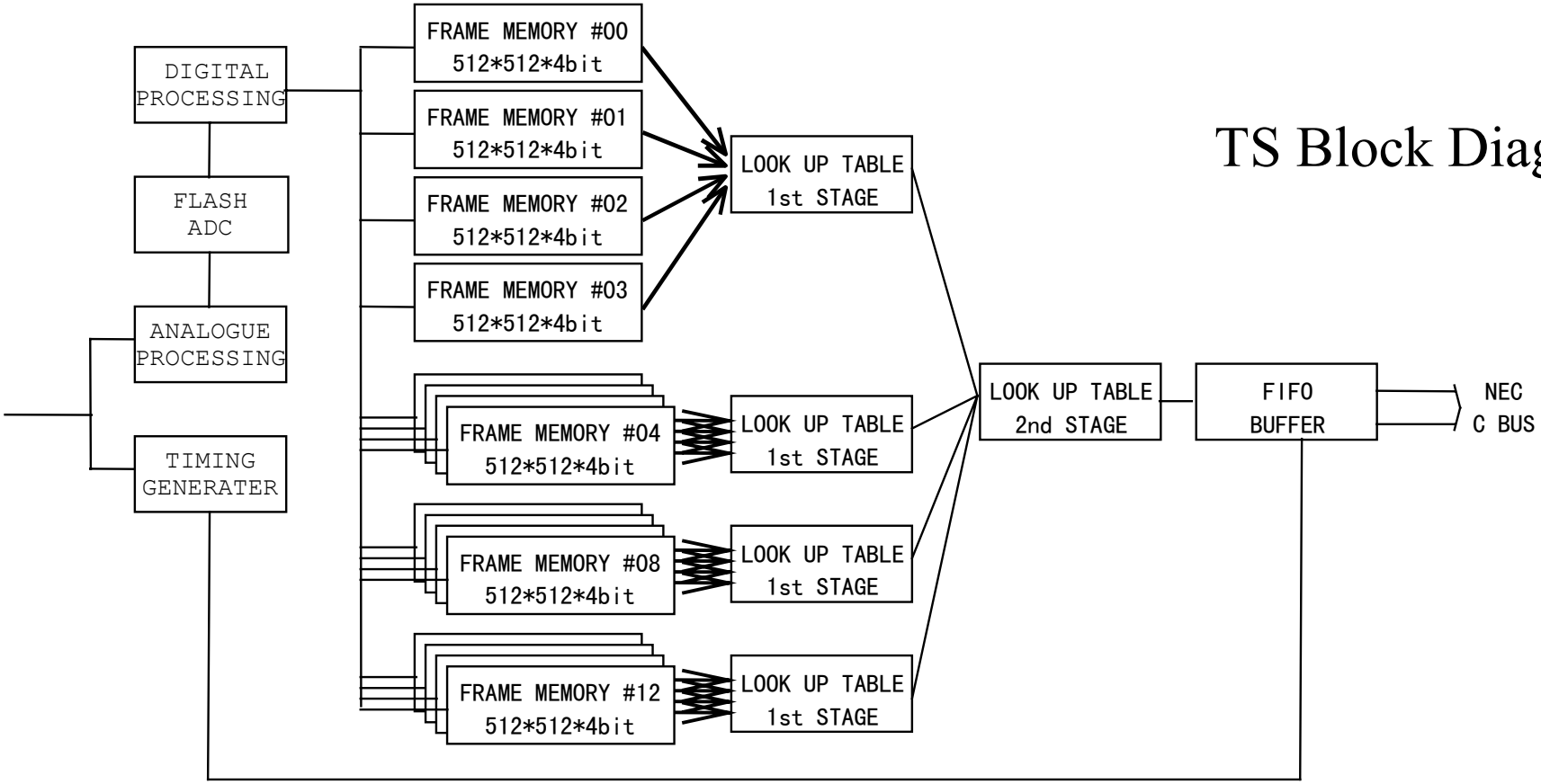
Track Selector (Practical)

Developed for CHORUS location in 1994.

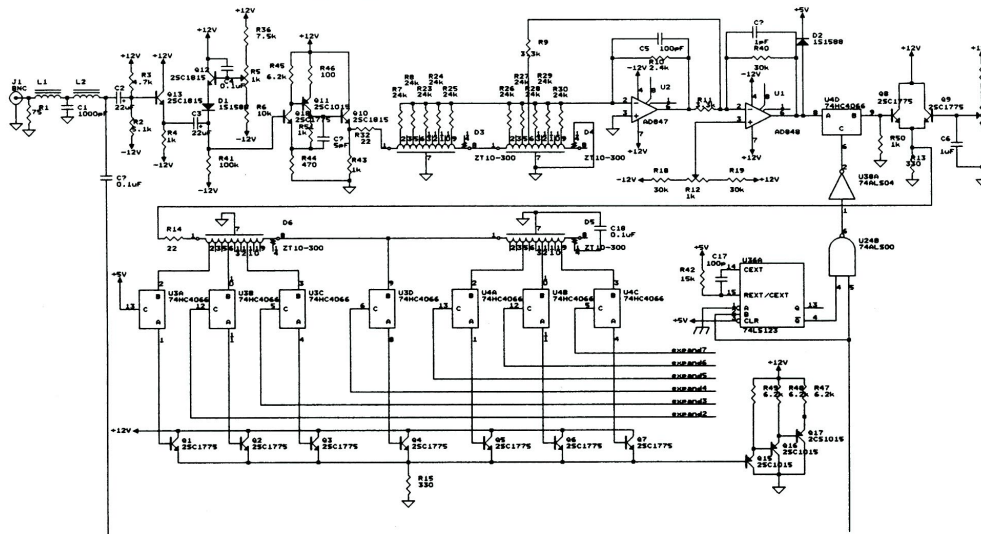
- CCD camera (NTSC 30fps)
  - ~1.2 sec for image data taking
  - Flash Xenon lamp was attempted to reduce data taking time.
- Stage was controlled by DOMS
  - DC servo motor.
  - 1~2 sec to move to the next view.
- Designed with TTL+VRAM
  - 15 trials/sec (@10MHz clock)

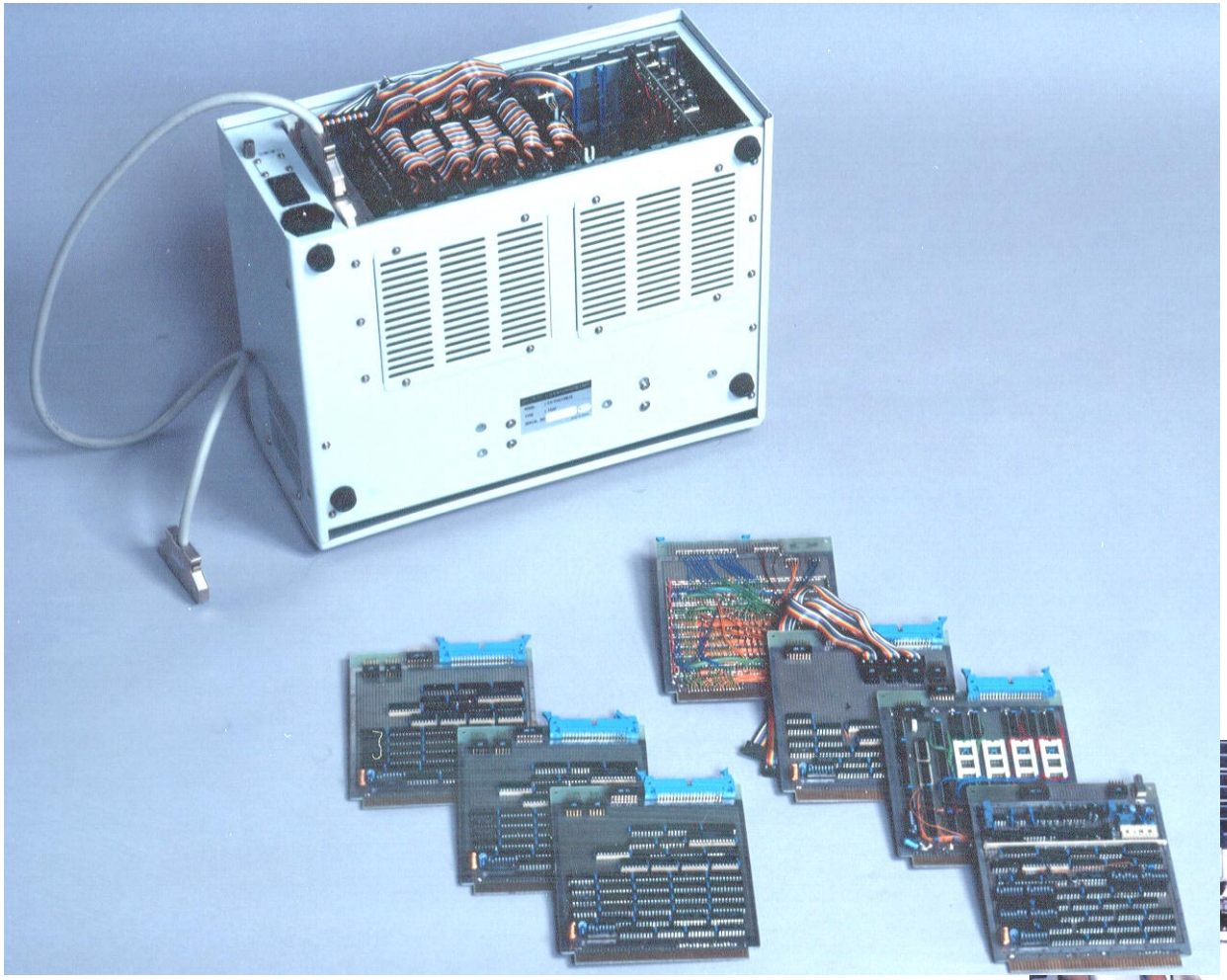
$\Rightarrow$ 0.3 views/sec for predicted angle

TS Block Diagram



Filter Circuit





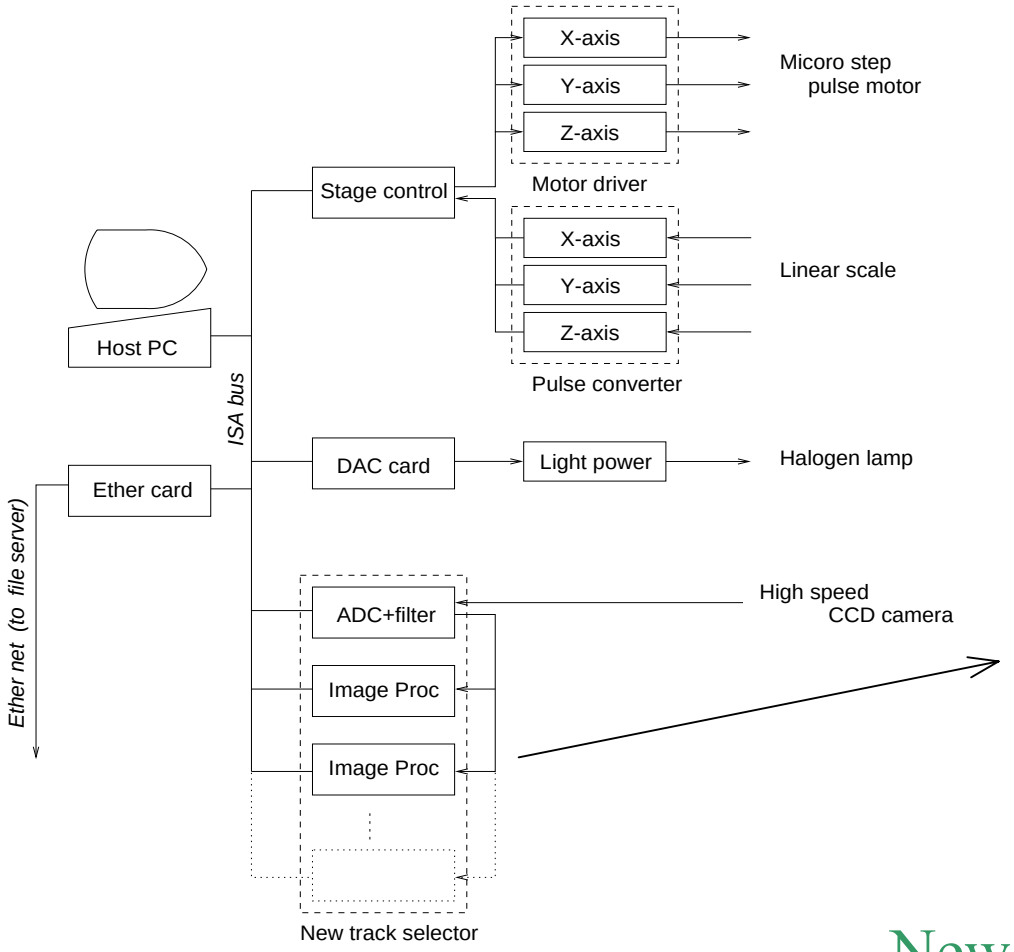
New Track Selector

Developed to speed up CHORUS location in 1996

- Fast CCD camera (120 fps)
  - ~0.16 sec for image data taking by using Electrical Shutter (1~4msec).
- Stage was driven by micro step motors.
  - 0.14~ sec to move to the next view.
- Designed with CPLD+SRAM
  - 90 trials/sec･board (@20MHz), Max. 8 boards/system

$\Rightarrow$ 3 views/sec for predicted angle

0.25 views/sec for all angle ($|\theta| < 0.4$, 8 boards)



New scanning system block diagram

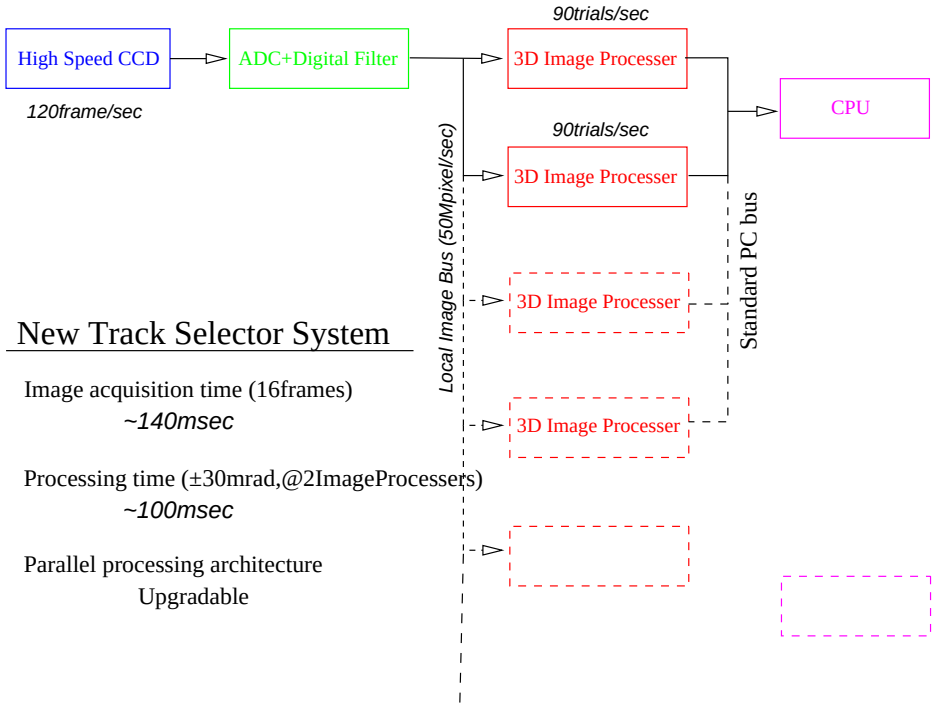
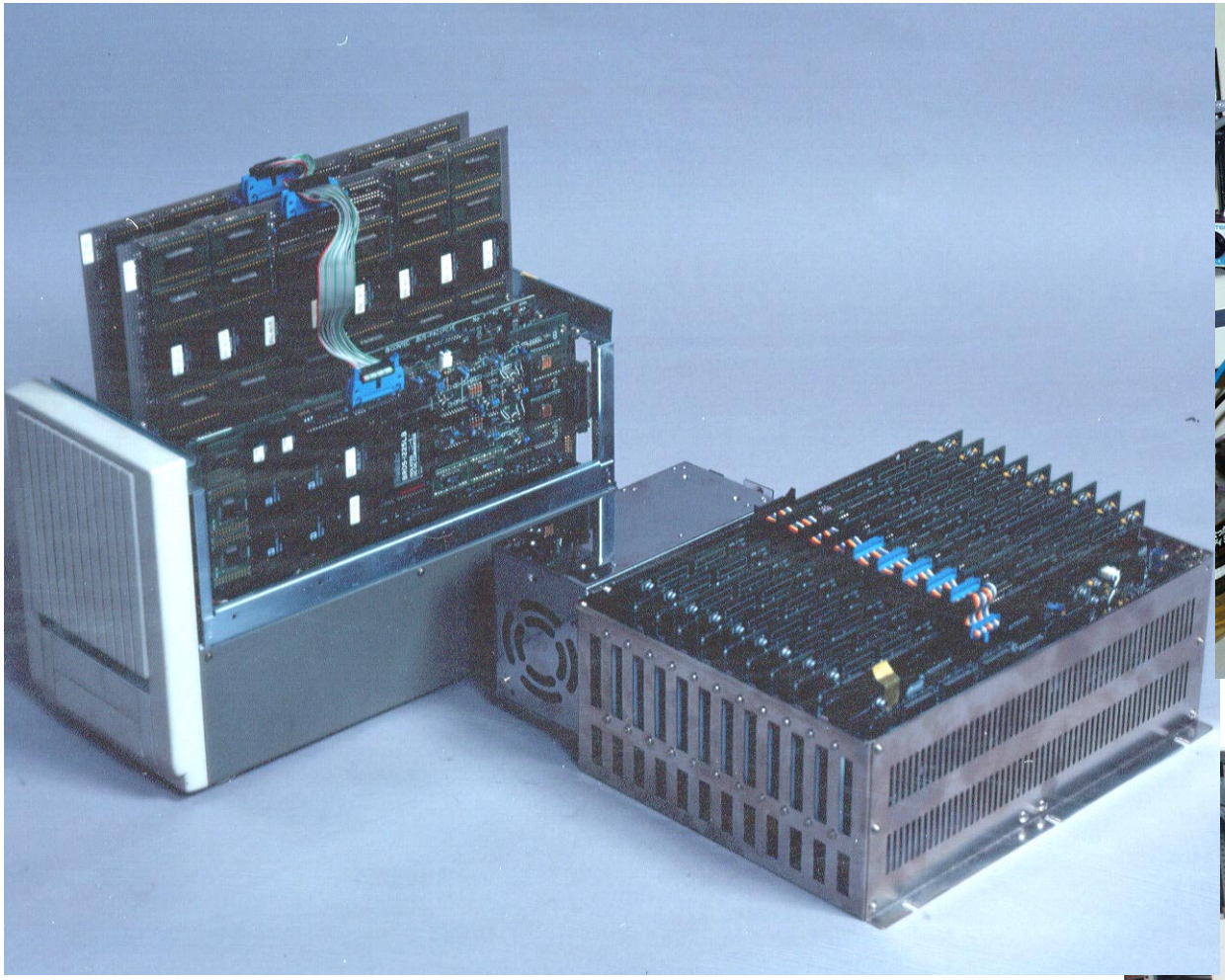
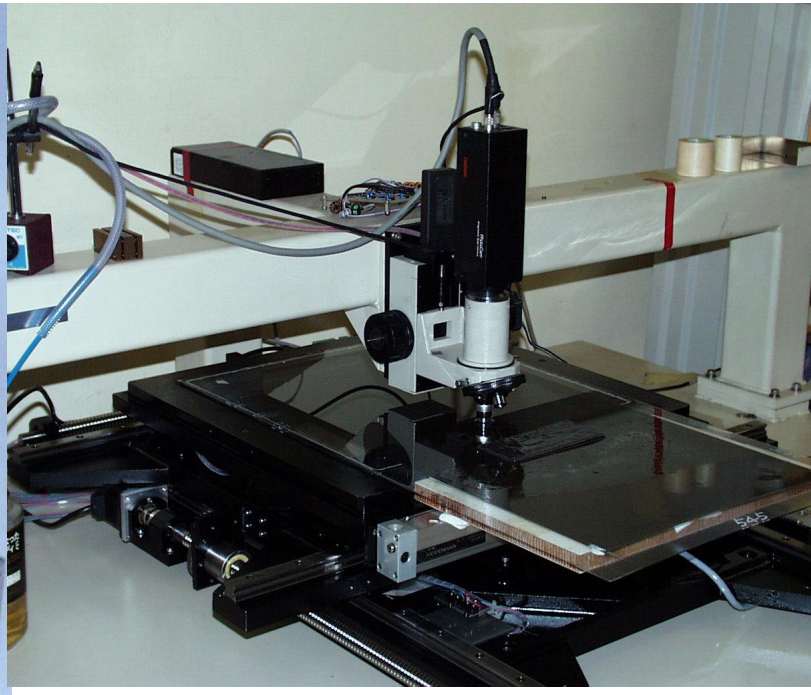
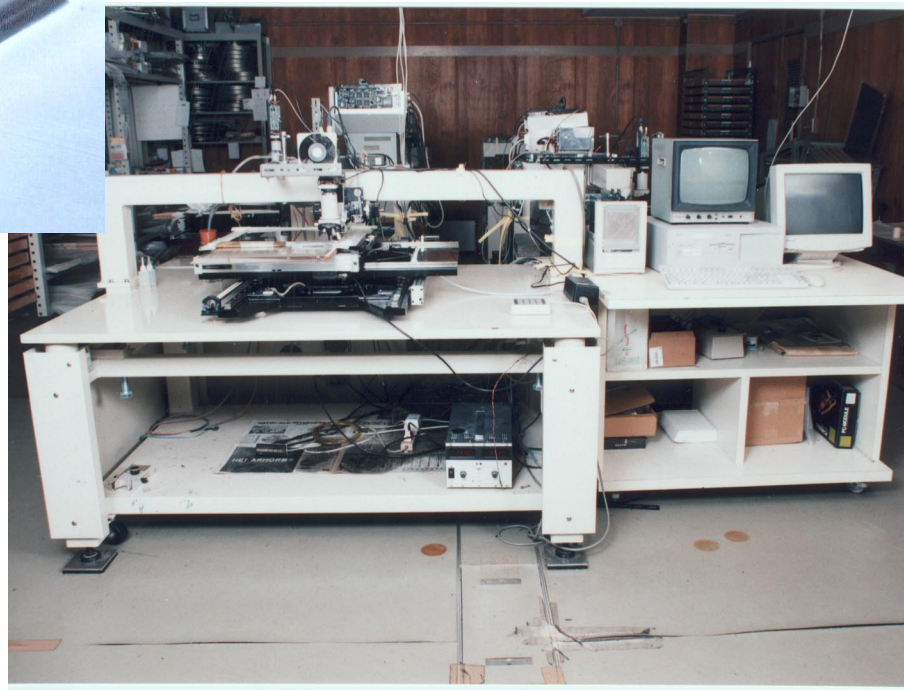


Image Processor

New Track Selector System Block Diagram







Ultra Track Selector

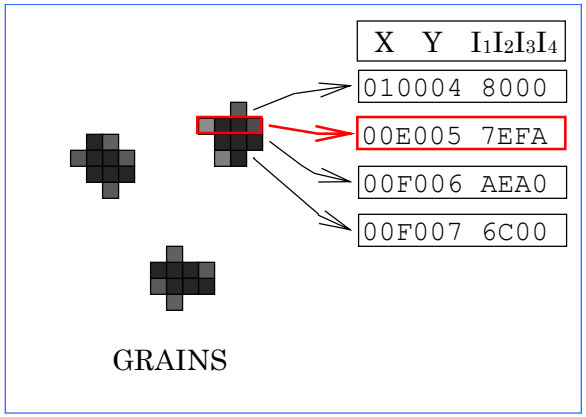
Developed for Netscan (DONUT,CHORUS II) in 1998

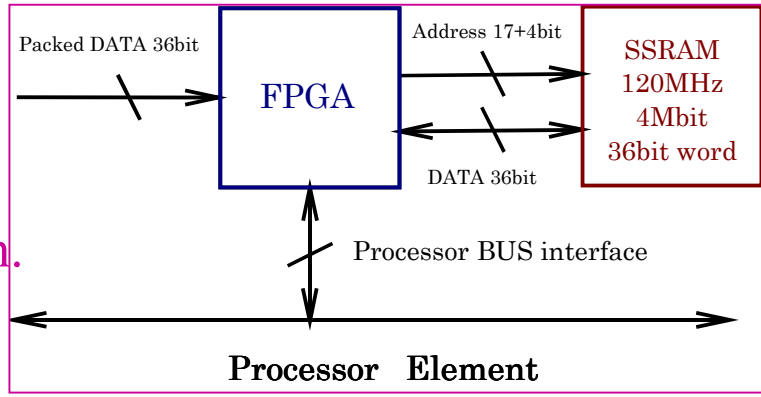
- Same CCD camera and stage control.
- New implementation of the track recognition.
  - Packed Pixel (Zero suppression).
- Designed with FPGA + Synchronous SRAM
  - 200 trials/sec·element (@120MHz), Max 50elements/system

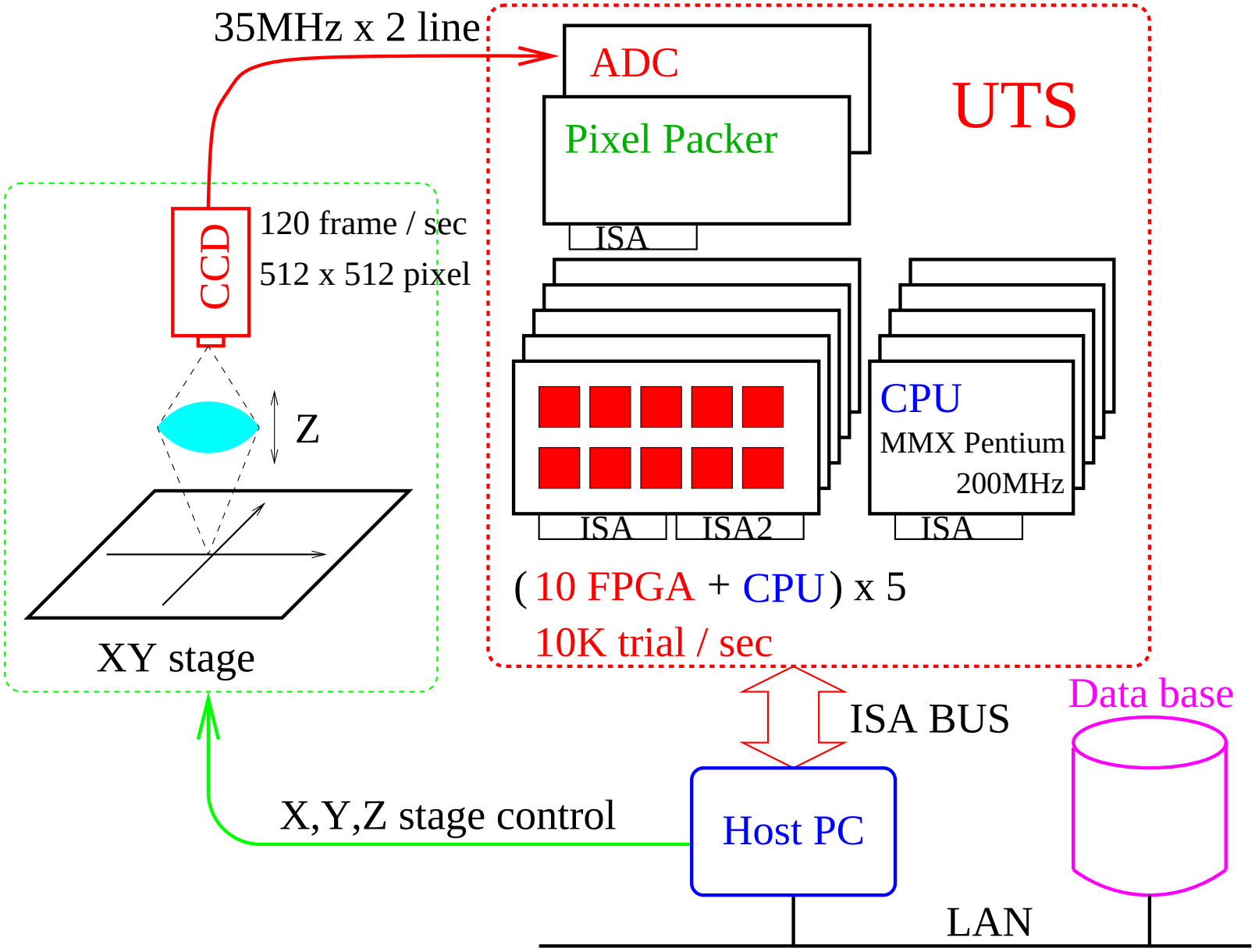
$\Rightarrow$ 3 views/sec for all angle ($|\theta| < 0.4$)

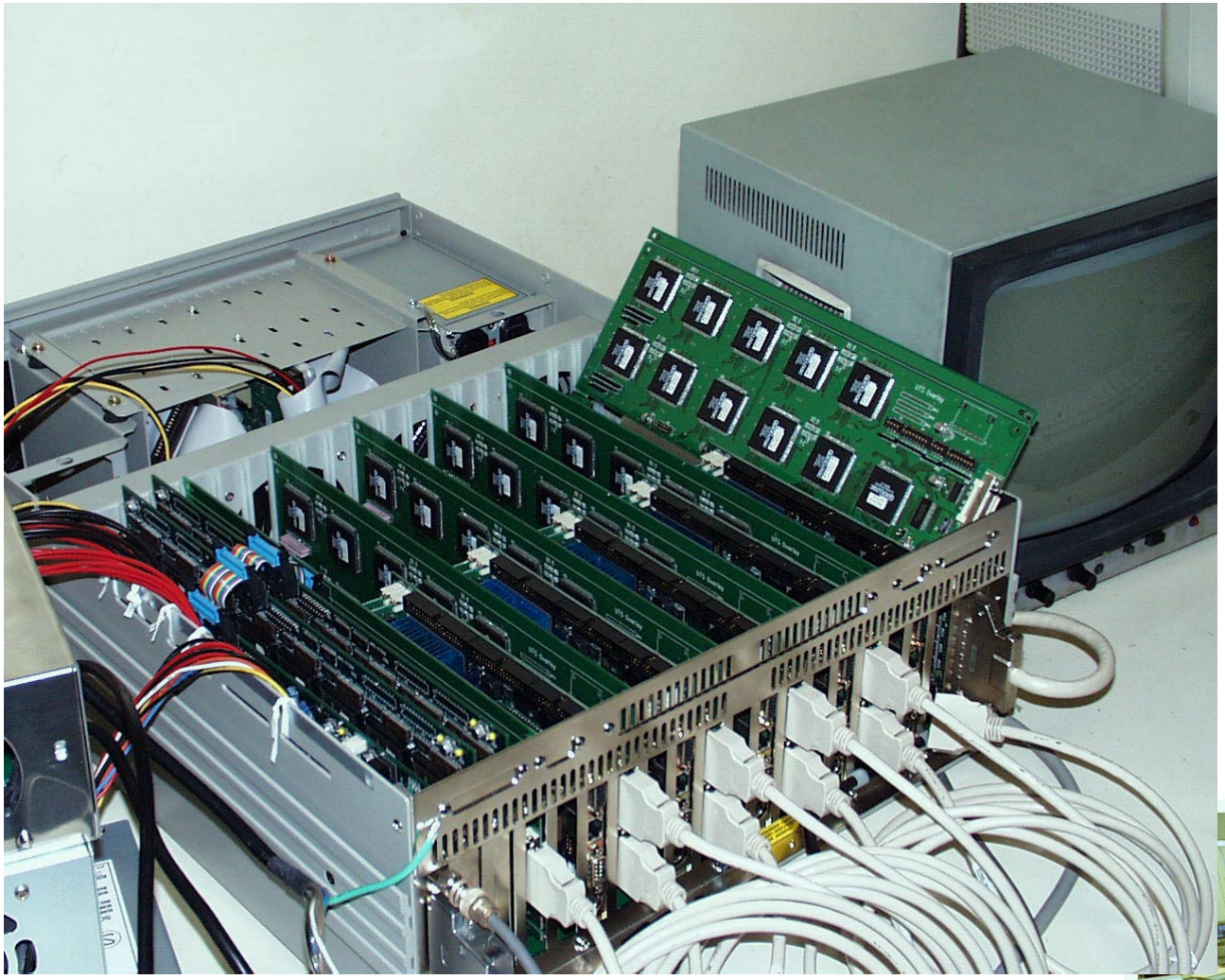
UTS Architecture

- Process zero suppressed pixel data.
  - Reduce data size down to 1/16
- Parallel processing with up to 50 elements.
  - Each element can process different angle space in parallel.
  - 480Mbyte memory bandwidth for each element. Total bandwidth ~ 24Gbyte/system.
  - SSRAM are used for working memory. NO dead cycle and 100% usability.






35MHz x 2 line
ADC
Pixel Packer
ISA
UTS
CCD
120 frame / sec
512 x 512 pixel
Z
CPU
MMX Pentium
200MHz
ISA
ISA2
ISA
(10 FPGA + CPU) x 5
10K trial / sec
XY stage
ISA BUS
Data base
X,Y,Z stage control
Host PC
LAN



UTS

Summary of the past scanning systems

- E531, WA75, (E653), etc . (~1994)
  - Semi-automatic scanning

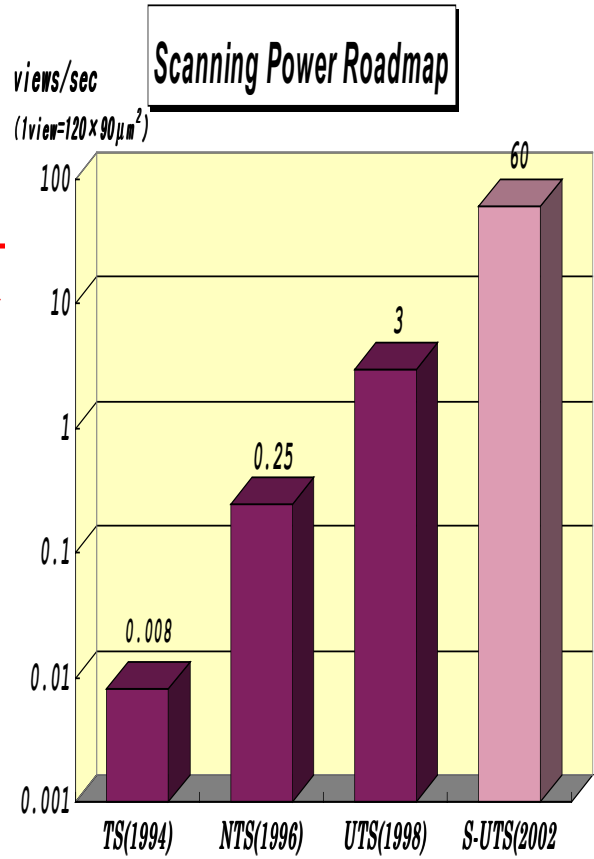
- CHORUS phase I Phys.Lett B497:8-22,2001
  - Track selector(1994~), New TS(1996~)

Automatic Scanning

→ Predicted angle and point scan.

- DONUT Phys.Lett B504:218-224,2001, CHORUS phase II
  - UTS (1998~) → Net scan (angle: $|\theta|<0.4$).

×100 processing power is required due to angle space



We need much more scanning power.

Next generation emulsion readout system 'S-UTS'

Over 20cm^2/hrs is required for OPERA etc.

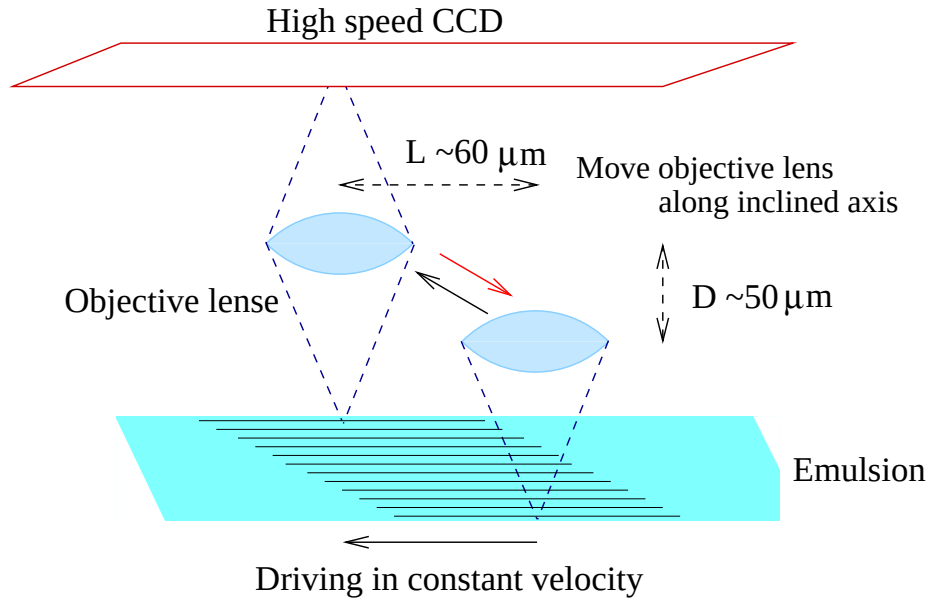
Image taking speed is an essential property.

The bottleneck is caused by

- Camera frame rate
  - ~130msec for a image set (16 frames) of a view with 120fps camera
- Mechanical response of stage
  - ~120msec is required for moving to and settling down the next view.

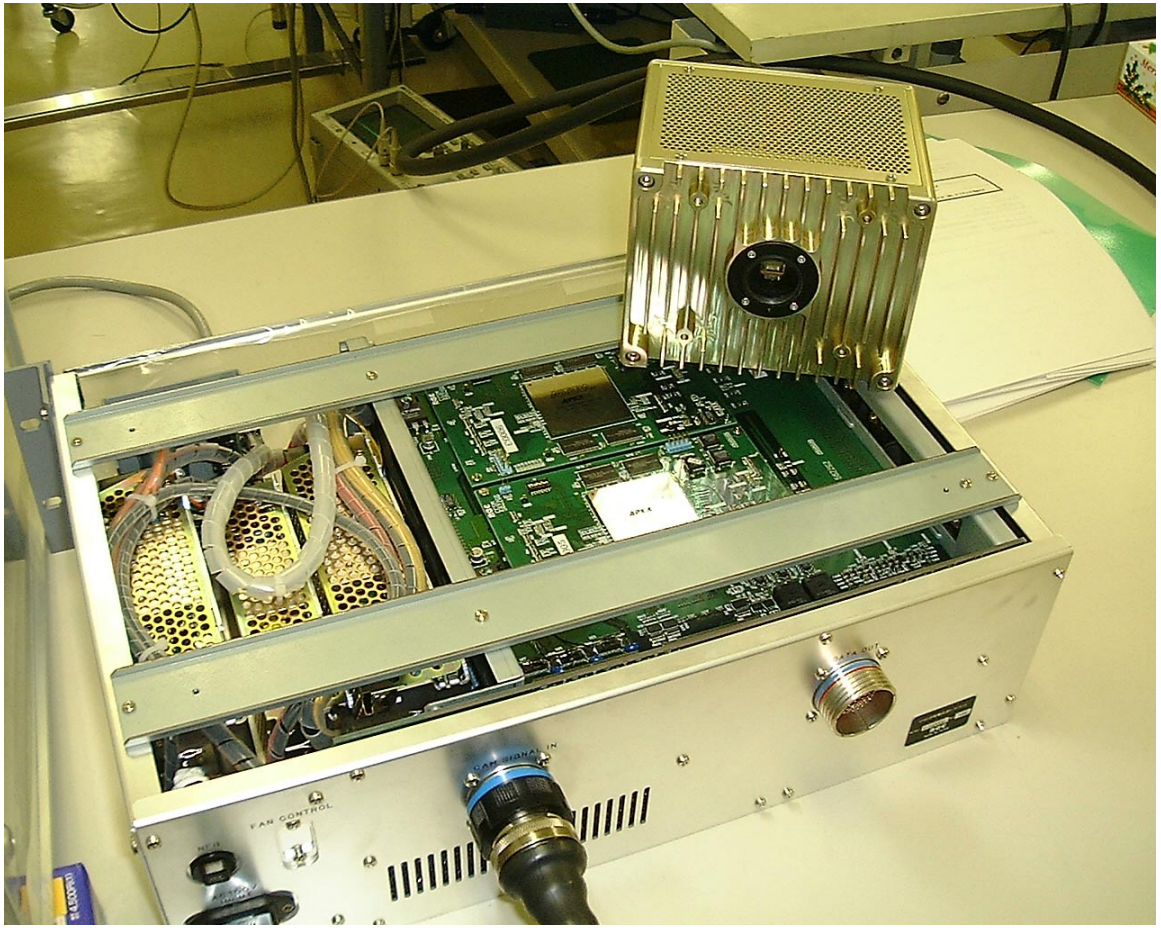
Non-stop image taking

- Ultra High Speed Camera
  - Up to 3k frames per second.
    → Max 100views/sec
- Image taking by follow shot
  - No go-stop operation to avoid a mechanical bottleneck.

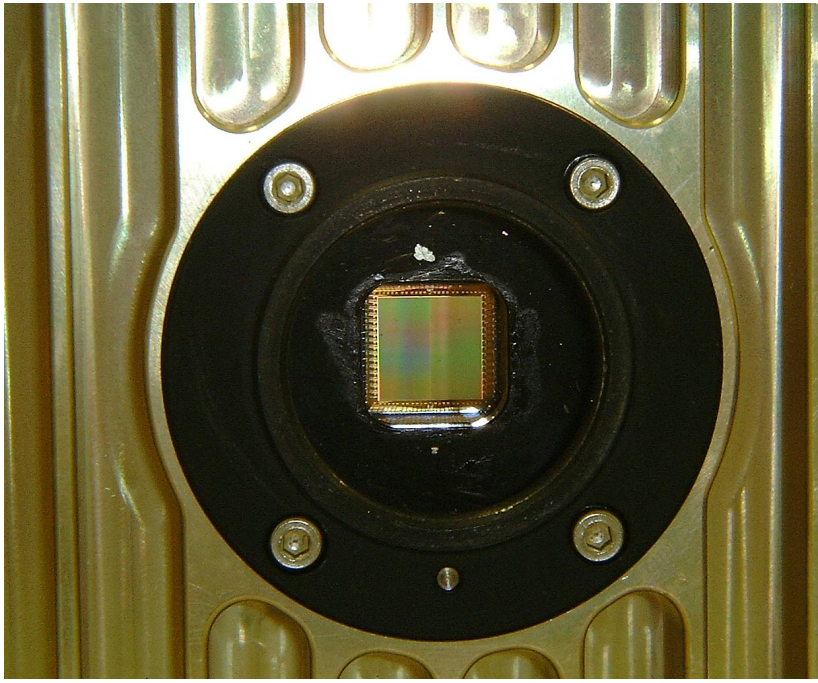


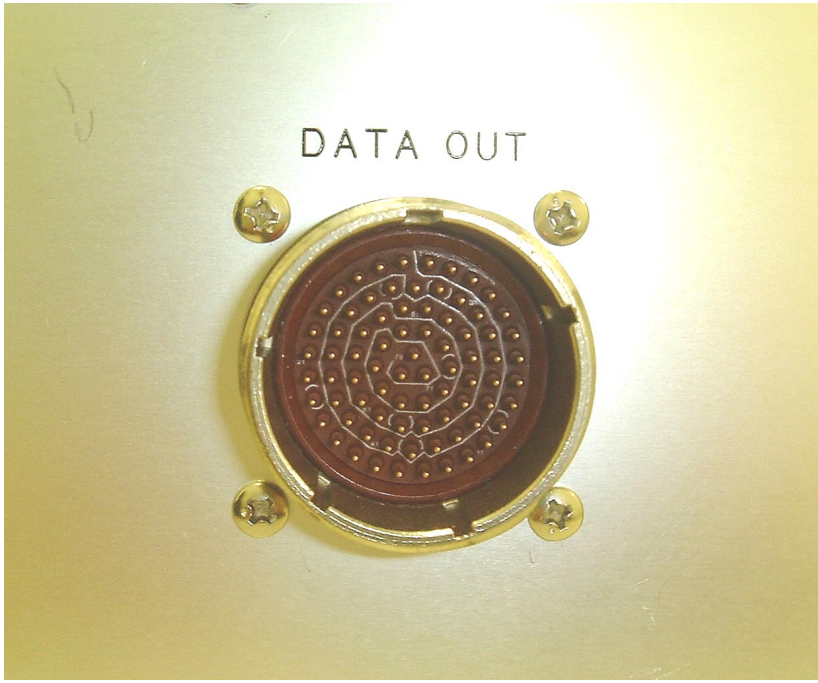
Ultra High Speed CCD Camera

- Ultra high speed image taking up to 3kfps.
  - 32(@40.32MHz) channel readout.
- Digital output via LVDS, 1.3GByte/sec.
  - Channel Link compatible driver ×6.
- Suitable for TIYODA ×50, $(170\mu m)^2$ of a view size
  - H512×V504 pixels, 17μm×17μm each pixel.
- Electrical Shutter for Exposure Control
  - Down to 10μsec and 1.2μsec step possible.



Camera Head + CCU





Ultra High Speed CCD Camera

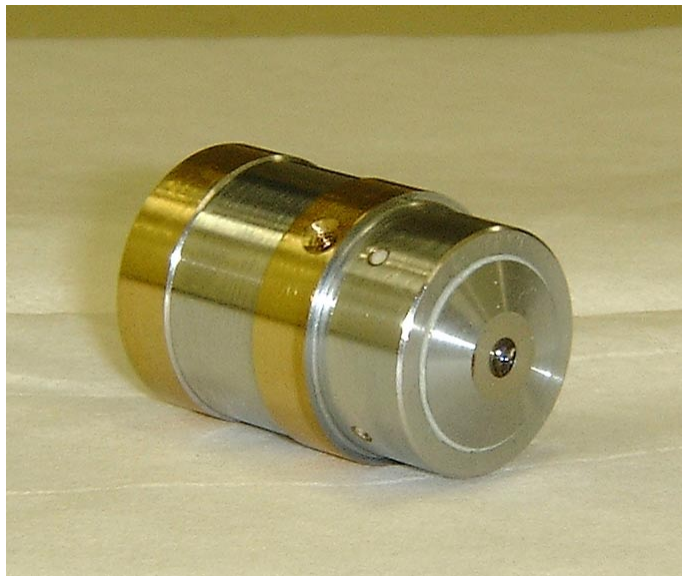
for S-UTS

Objective Lens Actuator System

Requirement

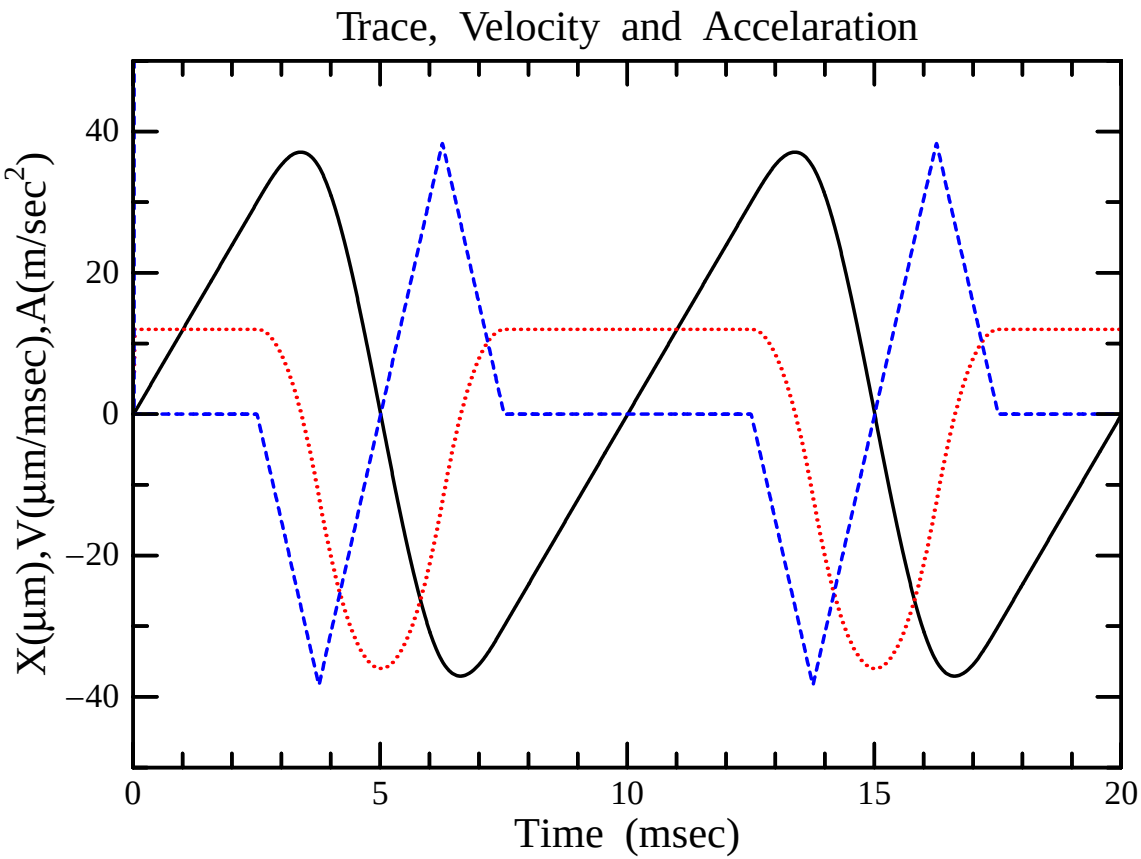
- Enough stroke (> a half view size)
- Accuracy ~sub-pixel size
- Linearity
- High resonant frequency (f_{res}>2kHz)

- Controlled by Piezo actuator
- Parallelogram flexure guiding

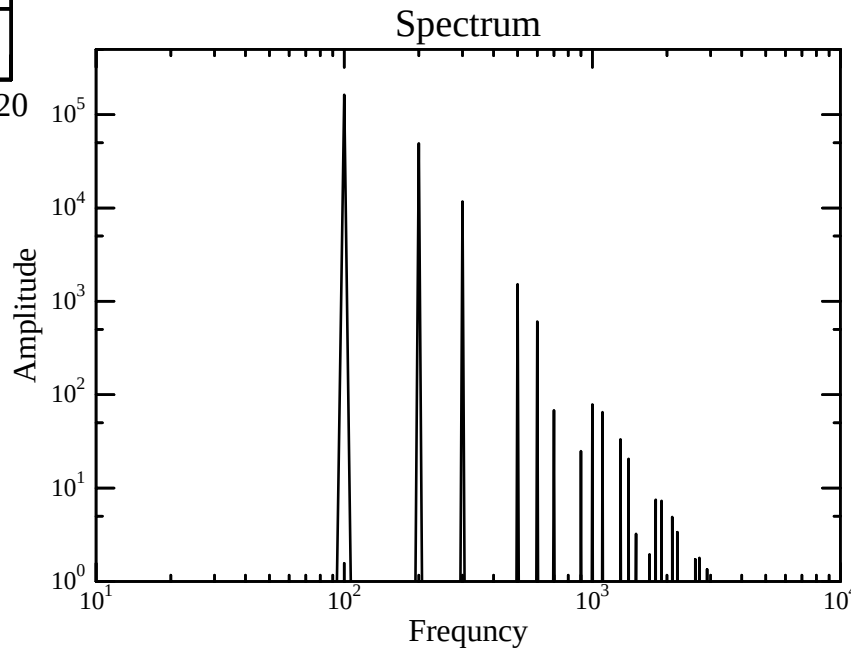


Objective lens core

D~16.4mm, W~13g



Trace of an ideal motion at 100Hz

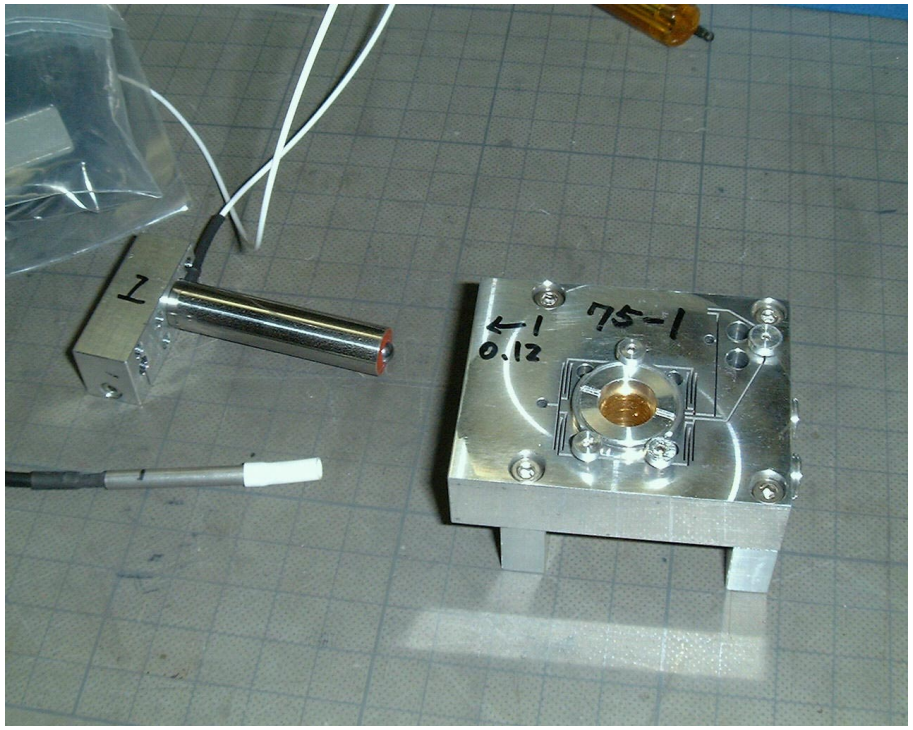


Spectrum of trace

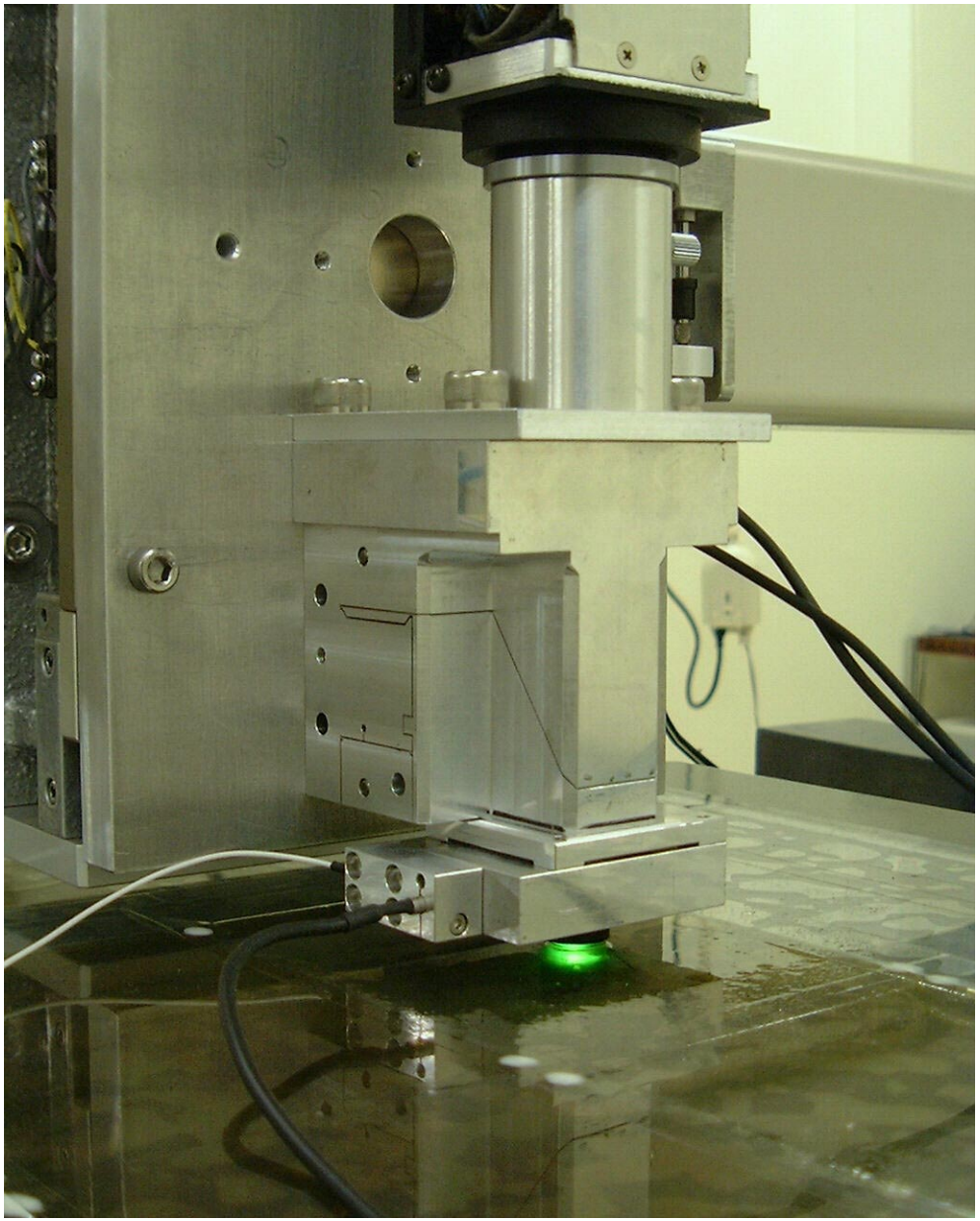
Objective lens actuators for S-UTS

Made by S.ISHIKAWA

Horizontal



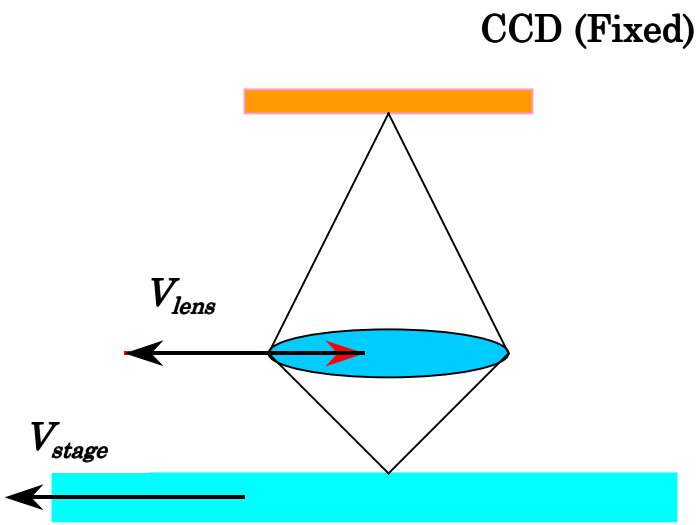
Horizontal + Vertical



Stage for S-UTS

S-UTS requires

- Good velocity uniformity for X-axis (basement).
  - Uniformity should be better than 0.3% at 10msec, 1% with shutter at least.



$|V_{lens}-V_{stage}| \times T <$ Pixel size

0.3% mismatch corresponding to 0.3μm positioning error in worst case .

Large mismatch causes image drifting.

$\Rightarrow$ Bad resolution and quality

- High rigidity rough positioning stage for Z-axis.
  - Stiffness ~ 10N/μm

    Expected force is 1N in horizontal, 10N in vertical.
- High rigidity or Large mass of Z-axis support.
  - Must support oscillating object at 60Hz or more.

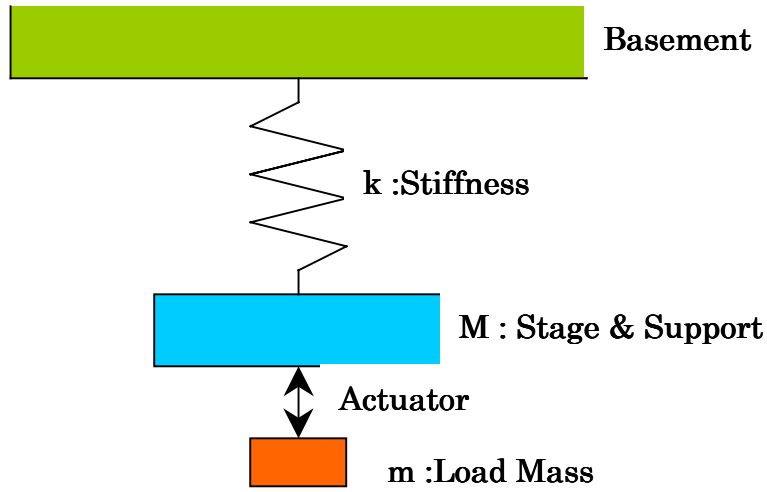
In case of Frequency < f_{res},

$\delta P \propto 1/k$ (k is stiffness)

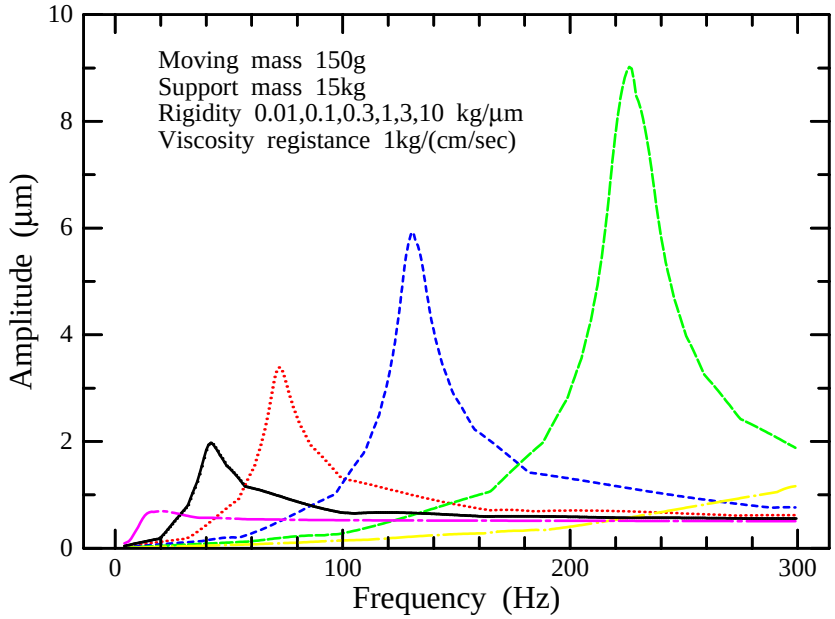
In case of Frequency > f_{res},

$\delta P \propto m_{load}/M_{stage}$

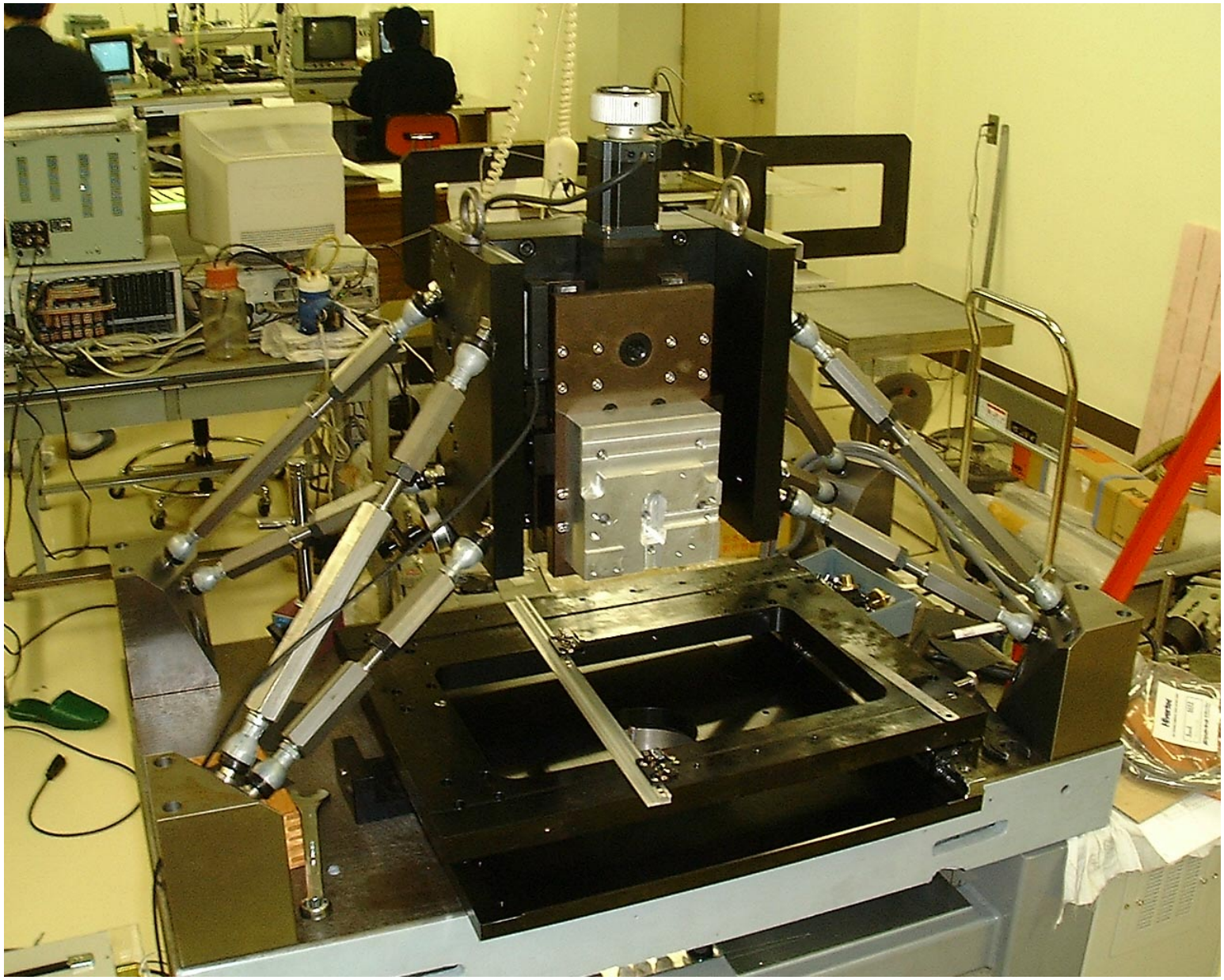
Operation frequency must not be equal to resonant frequency.



Preliminary Calculation



Amplitude at f_{res} is not reliable



Prototype stage for S-UTS by T.KAWAI

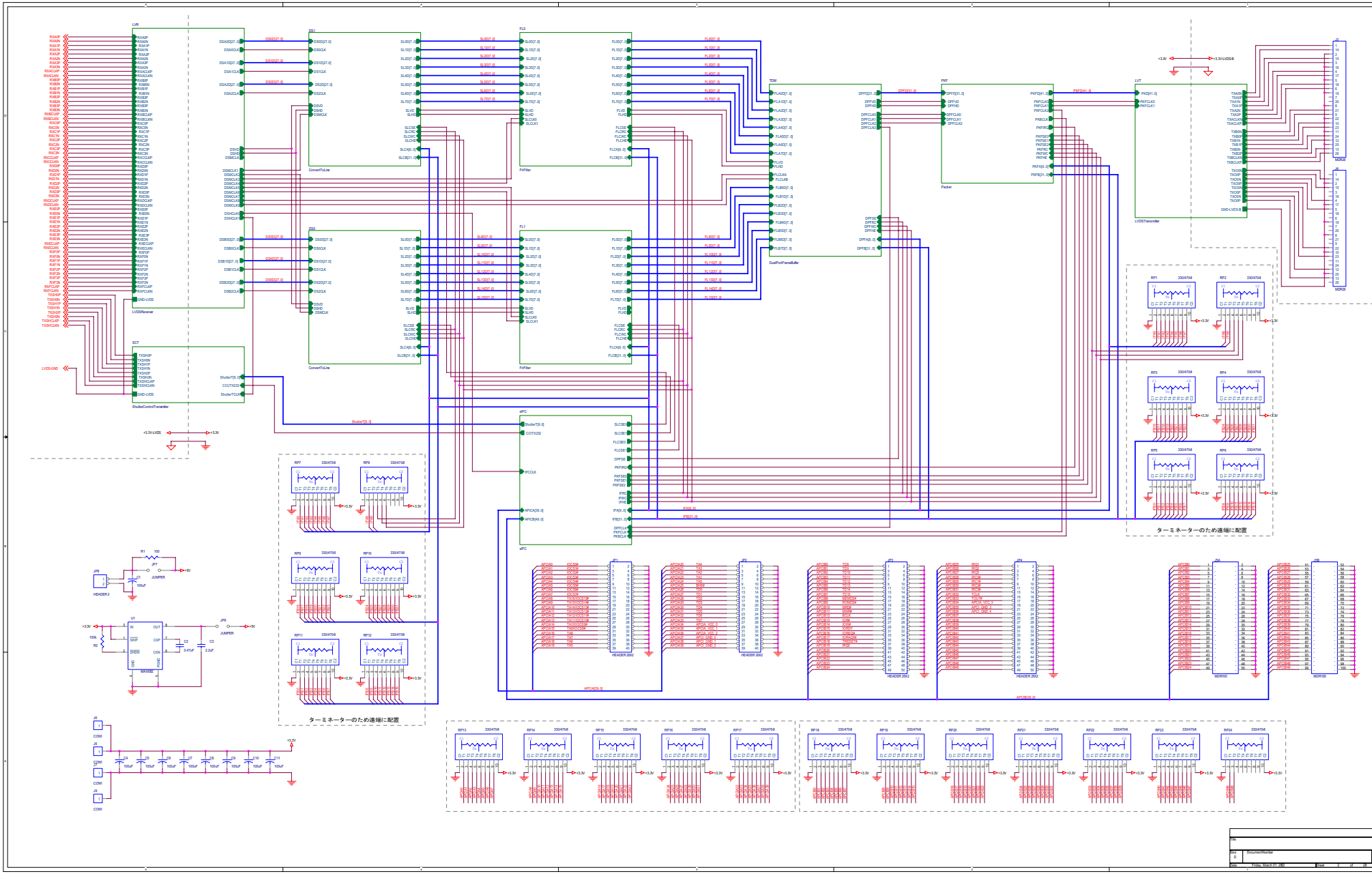
Image pre-processing (packing)

- The data from camera is very high data rate.
  - Peak data rate ~1.3Gbyte/sec ⇔ PCI is 133Mbyte/sec
  - Almost NO way to load on the PC's main memory in real time.
- Image taking system can not wait for processing.
  - The motion of lens and stage are synchronized tightly.

⇓

Larger scale hardware required

8ASIC FILTER+16FPGA+8DSSRAM



Pre-processor for S-UTS

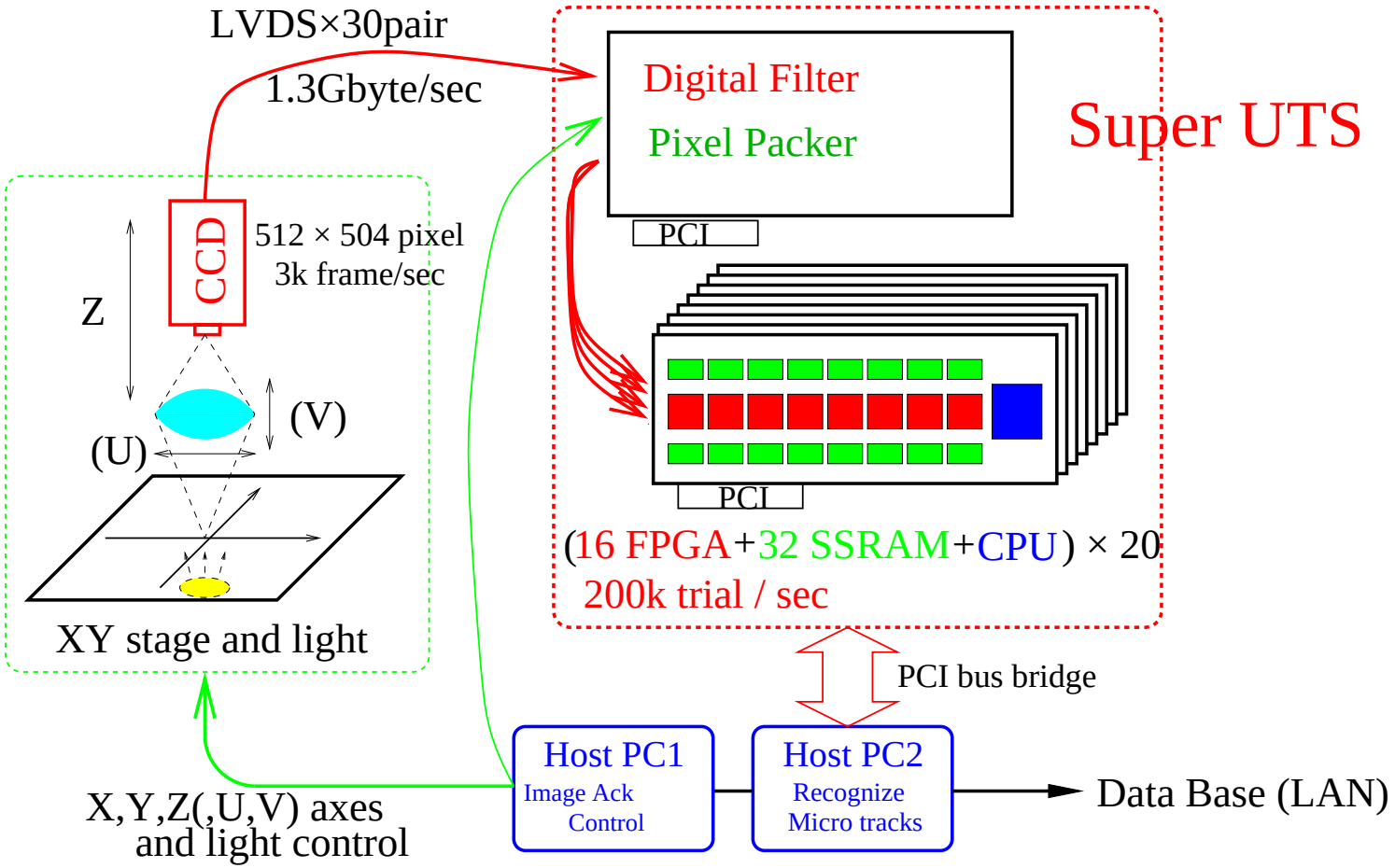
Track recognition by TS algorithm

Same strategy established in UTS will be applied.

To achieve ×20 recognition speed,

- Faster clock and twin engine on a processing element.
  - Main clock 120MHz → 200MHz. ×1.6
  - Two angles in parallel on an element. ×2.0
- Enlarge number of parallel processing
  - MAX 50 elements. → Over 300 elements. ×6

⇒ Total Memory Band Width = 480GByte/sec


LVDS×30pair
1.3Gbyte/sec
Digital Filter
Pixel Packer
Super UTS
CCD
512 × 504 pixel
3k frame/sec
Z
(V)
(U)
PCI
PCI
(16 FPGA+32 SSRAM+CPU) × 20
200k trial / sec
XY stage and light
PCI bus bridge
Host PC1
Image Ack
Control
Host PC2
Recognize
Micro tracks
Data Base (LAN)
X,Y,Z(,U,V) axes
and light control

Summary and Prospect

- The performance of S-UTS will achieve 40cm^2/hr.
  - 60views/sec, the effective view size is (140μm)^2.
- Status of development S-UTS
  - Prototype of Objective lens actuator and stage is almost ready.
  - Image Pre-processor of S-UTS will be ordered to the assembling company soon.
  - The detail design of S-UTS Processor will be started.
- Estimated Cost
  - 6M:camera + 4M:stage + 10M:electronics = 20M yen for prototype
  - However, the cost depend on the number of stage.

Dynamic Control Test

- Applied Feedback Control.
- The deviations from the ideal traces are less than 0.3μm at 60Hz.
- To maximize the data acquisition speed, 100views/sec, the control algorithm should be improved.